

FIG.1 PRIOR ART

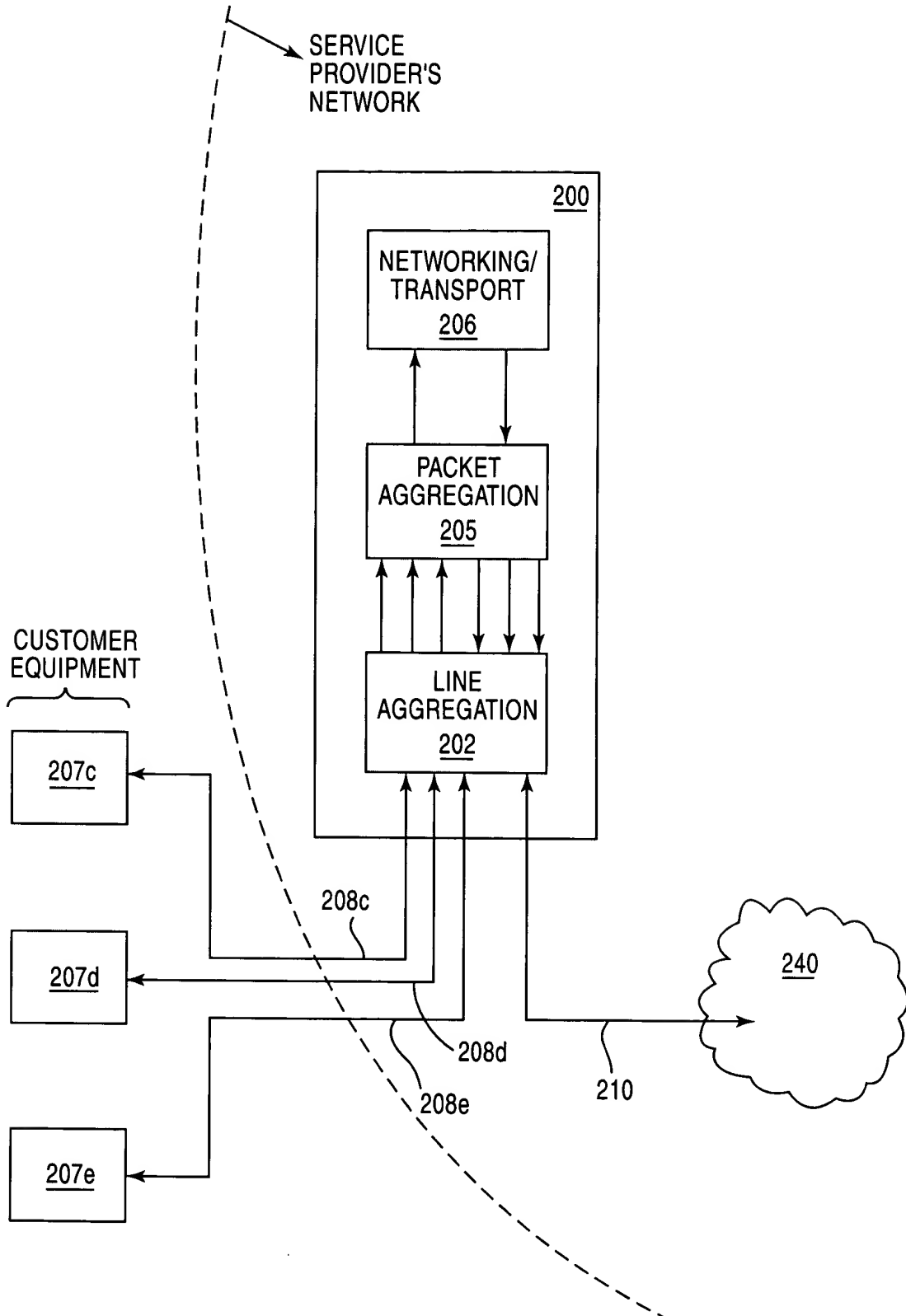


FIG.2A



Replacement Sheet

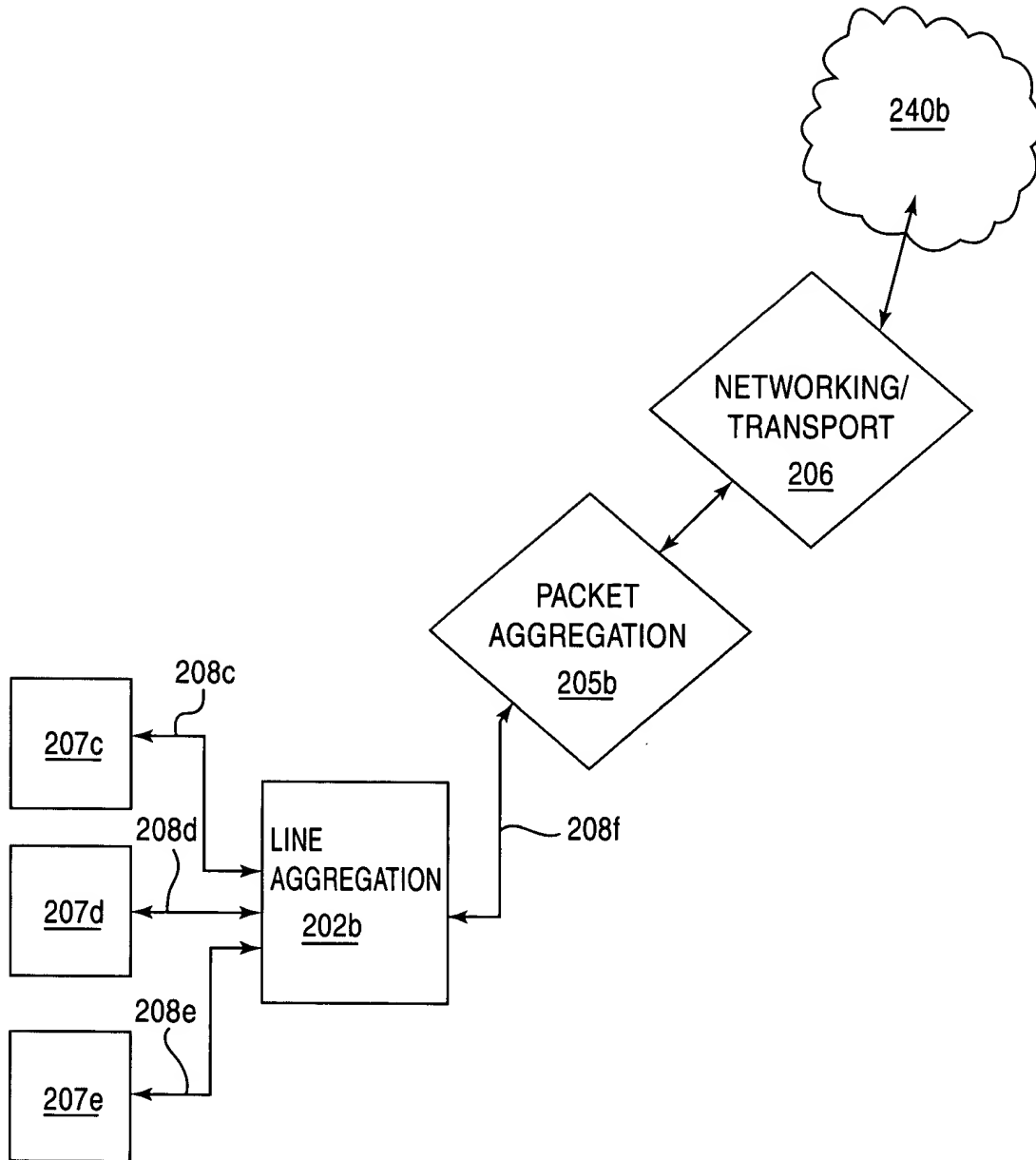


FIG.2b

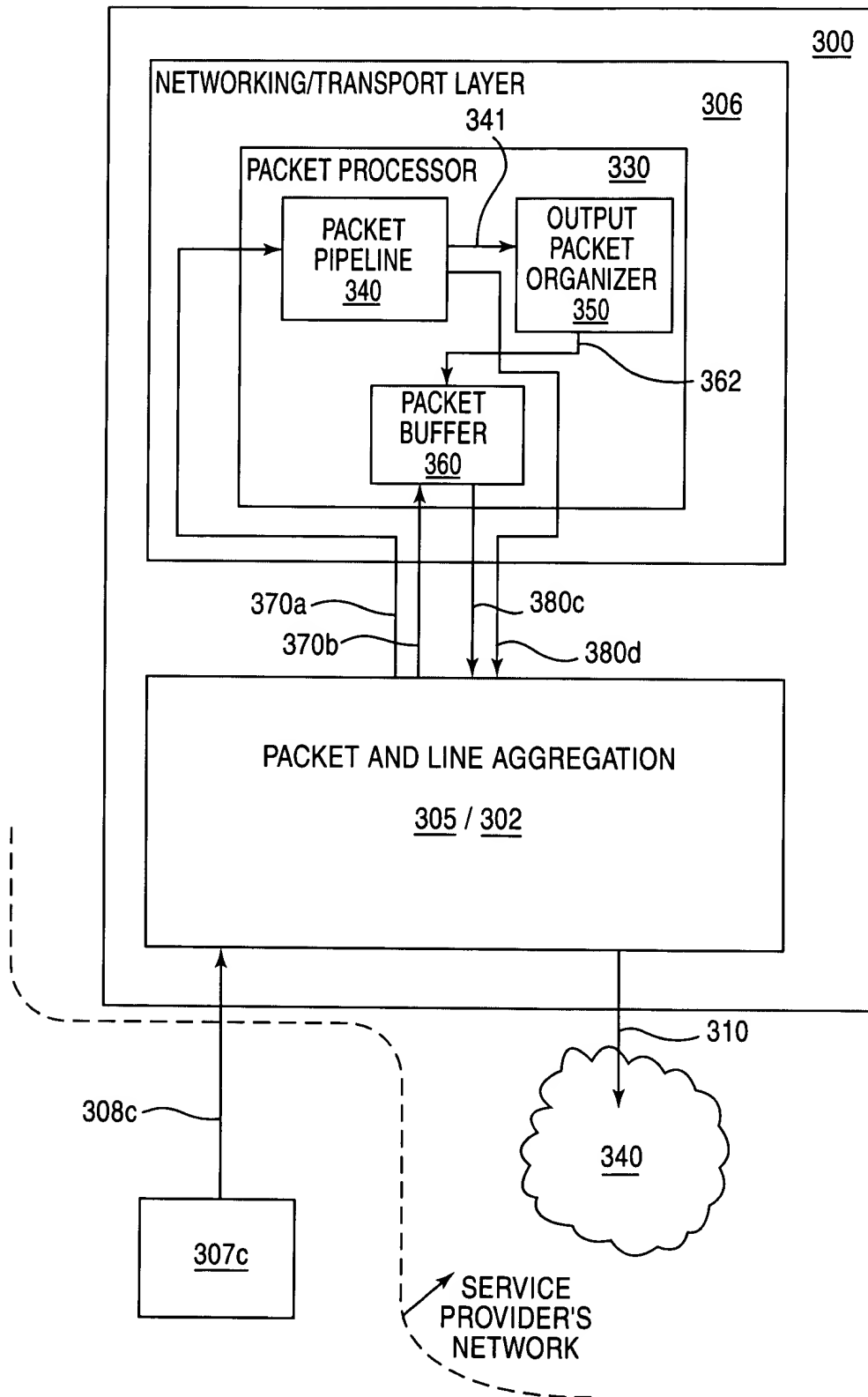


FIG.3A

FIG.3B

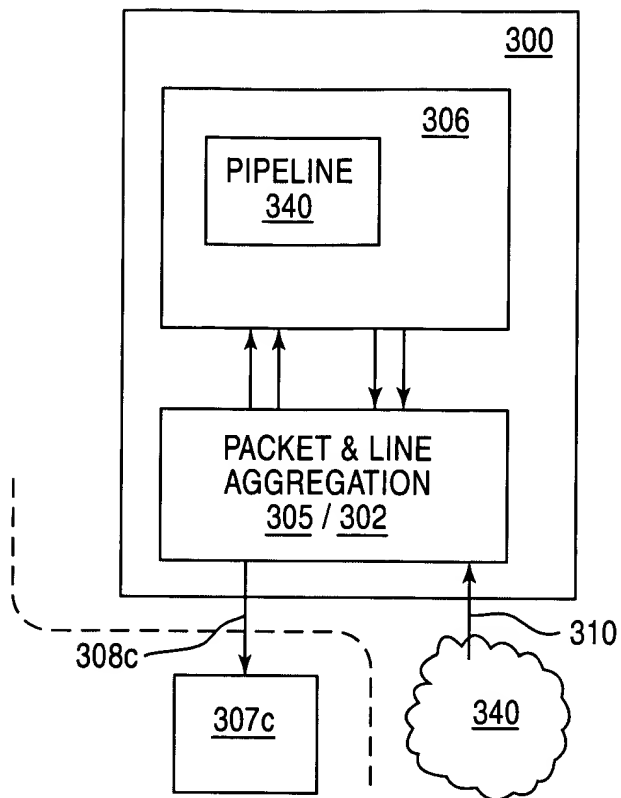
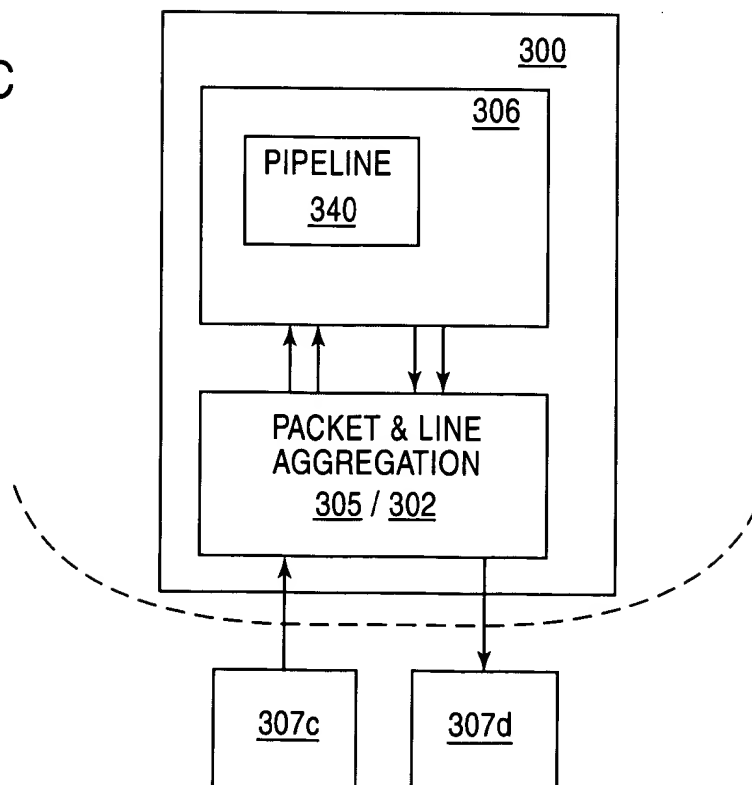
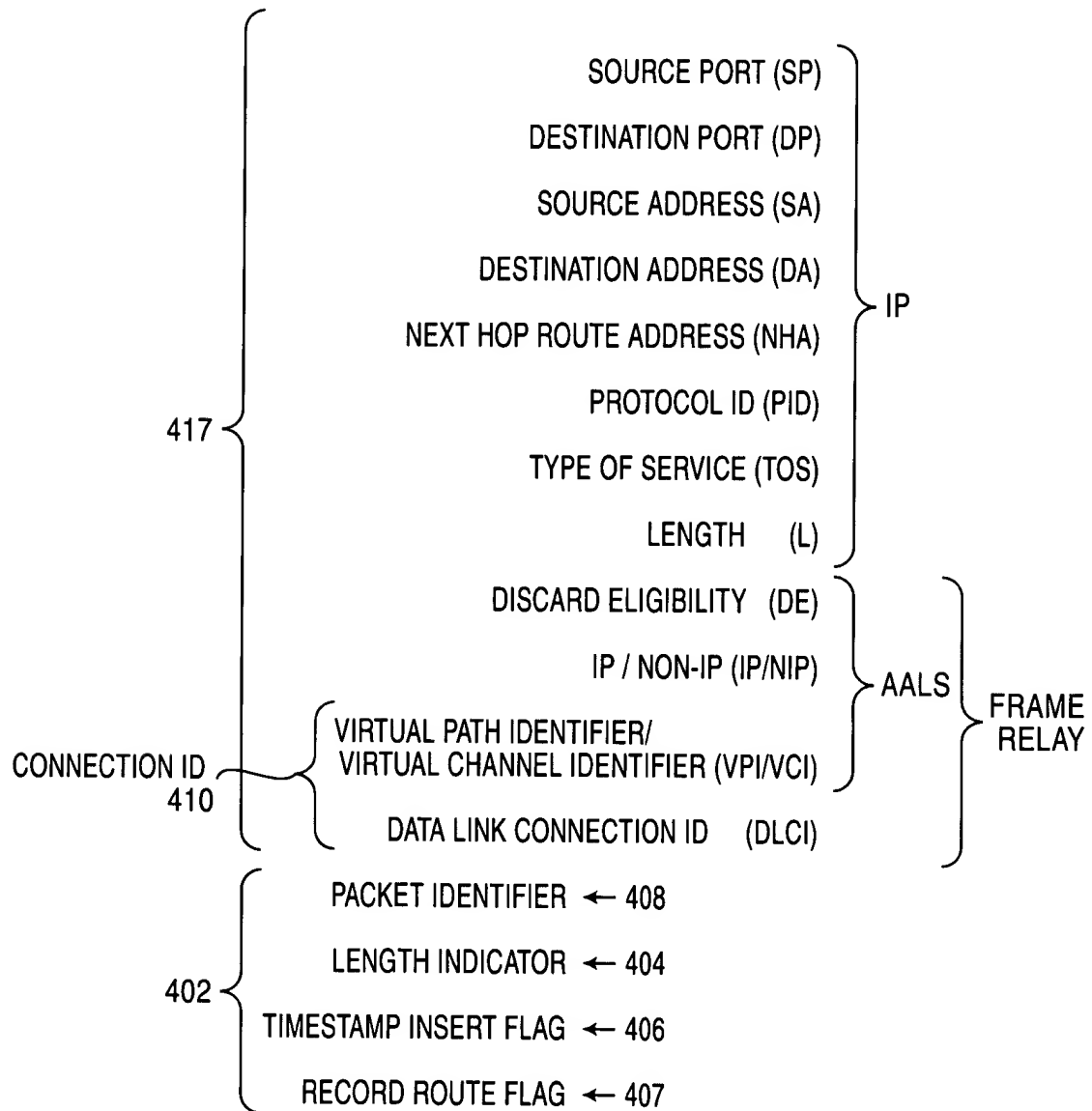


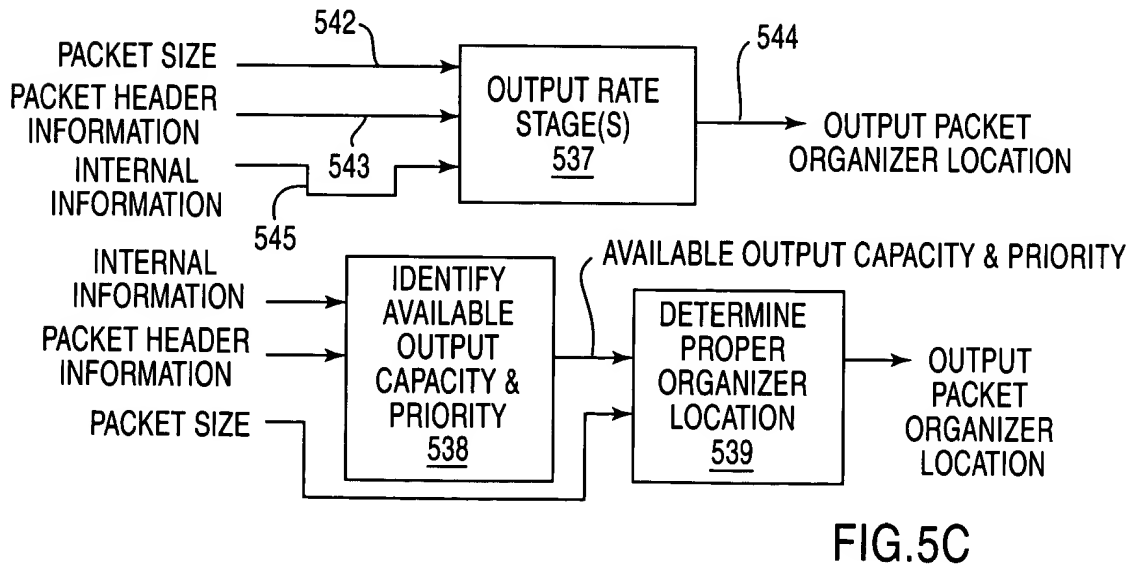
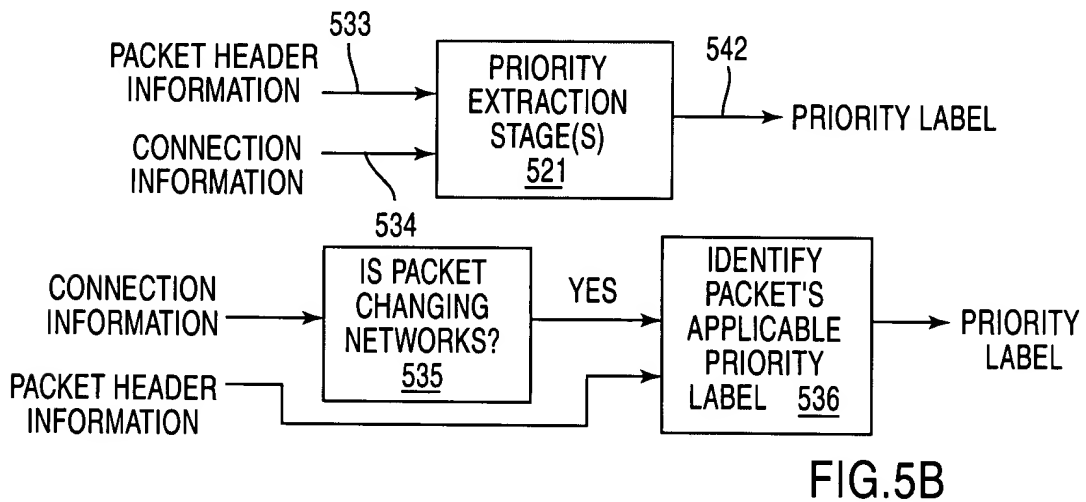
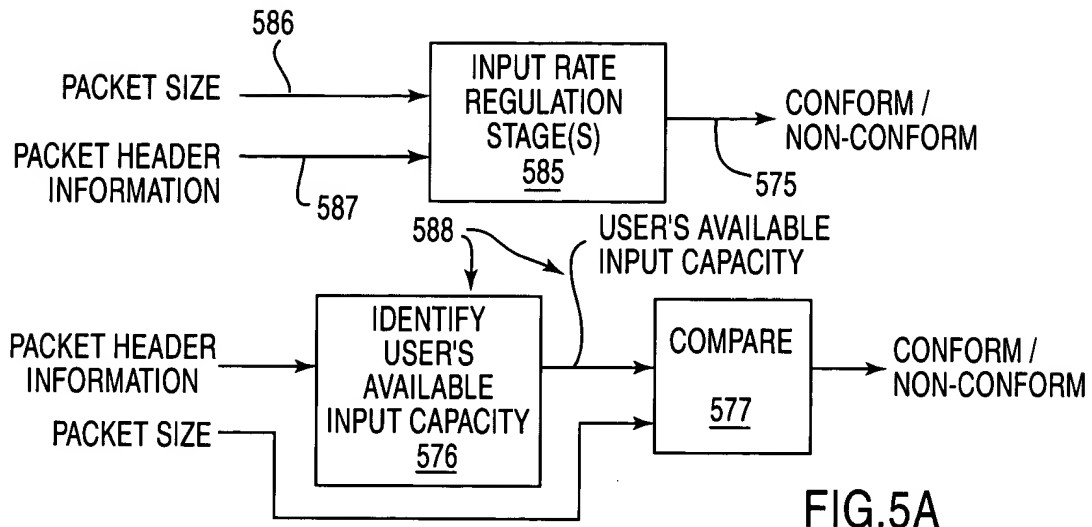
FIG.3C





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FIG.4



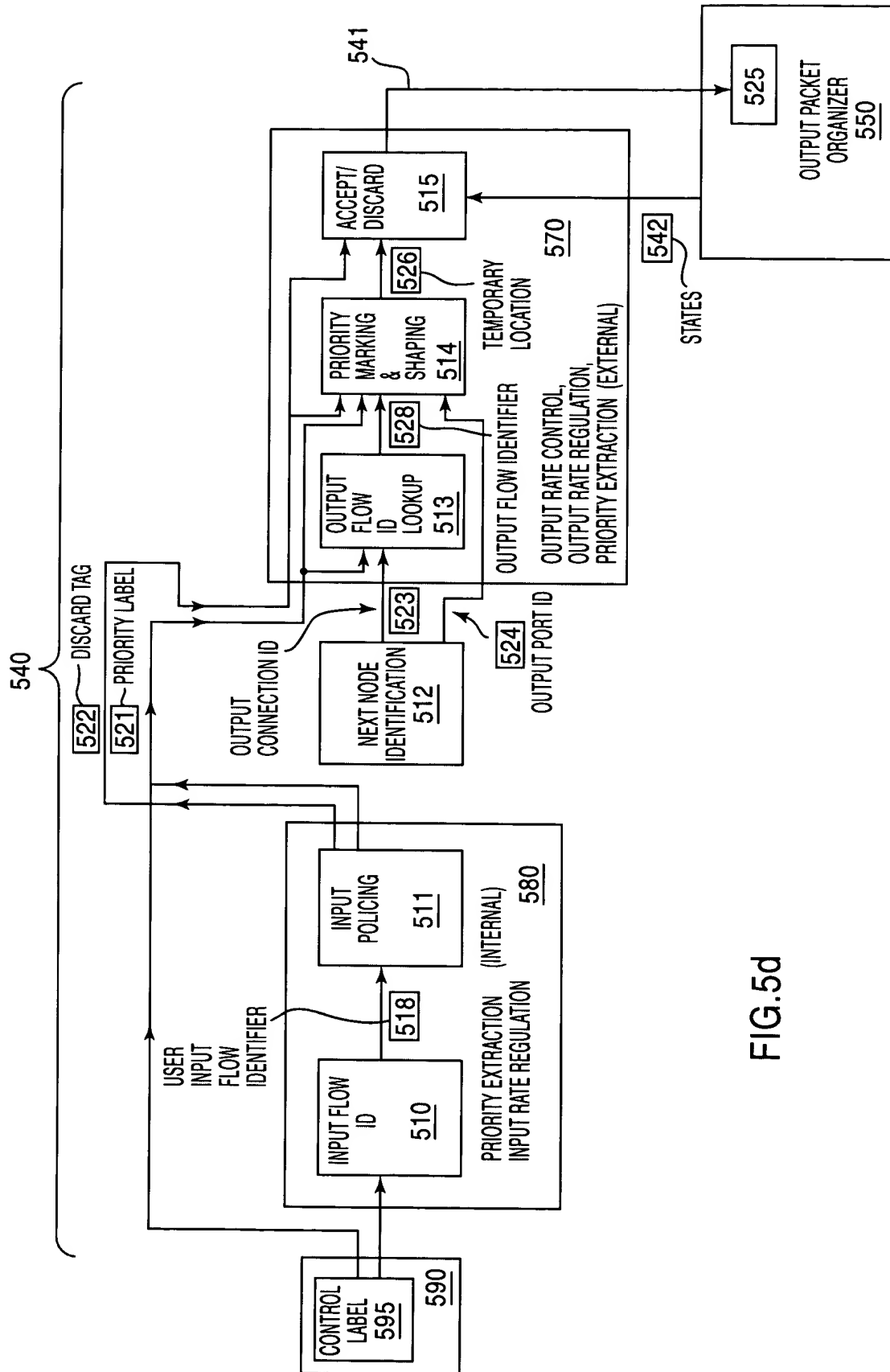


FIG. 5d

	INPUT FLOW ID STAGE	INPUT POLICING STAGE	NEXT NODE IDENTIFICATION STAGE	OUTPUT FLOW ID STAGE	PRIORITY MARKING AND SHAPING STAGE	ACCEPT/DISCARD STAGE
FIG.6A	X	X	X		X	X
FIG.6B			X	X	X	X
FIG.6C	X	X	X	X	X	X
FIG.6D			X		X	X

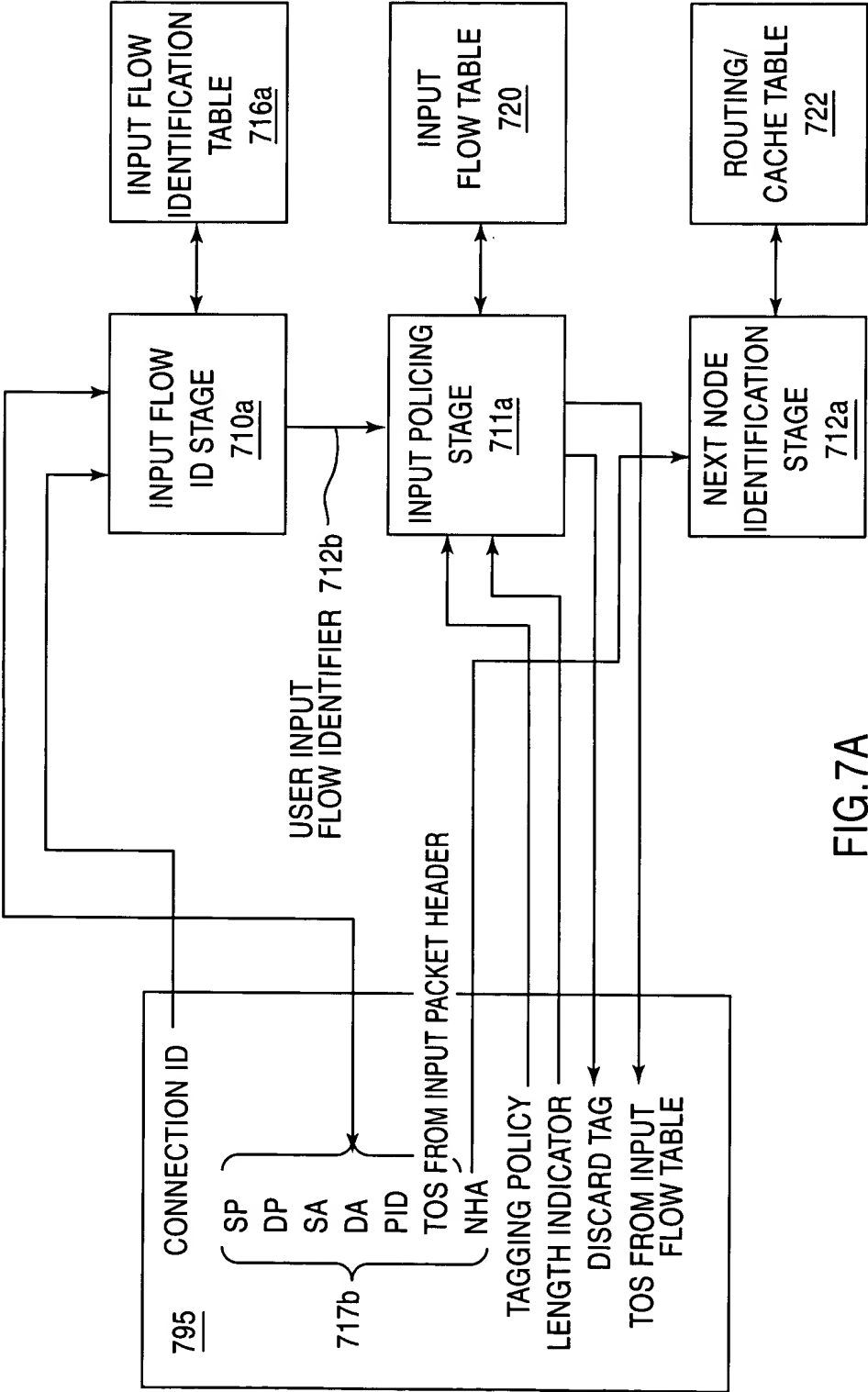


FIG. 7A

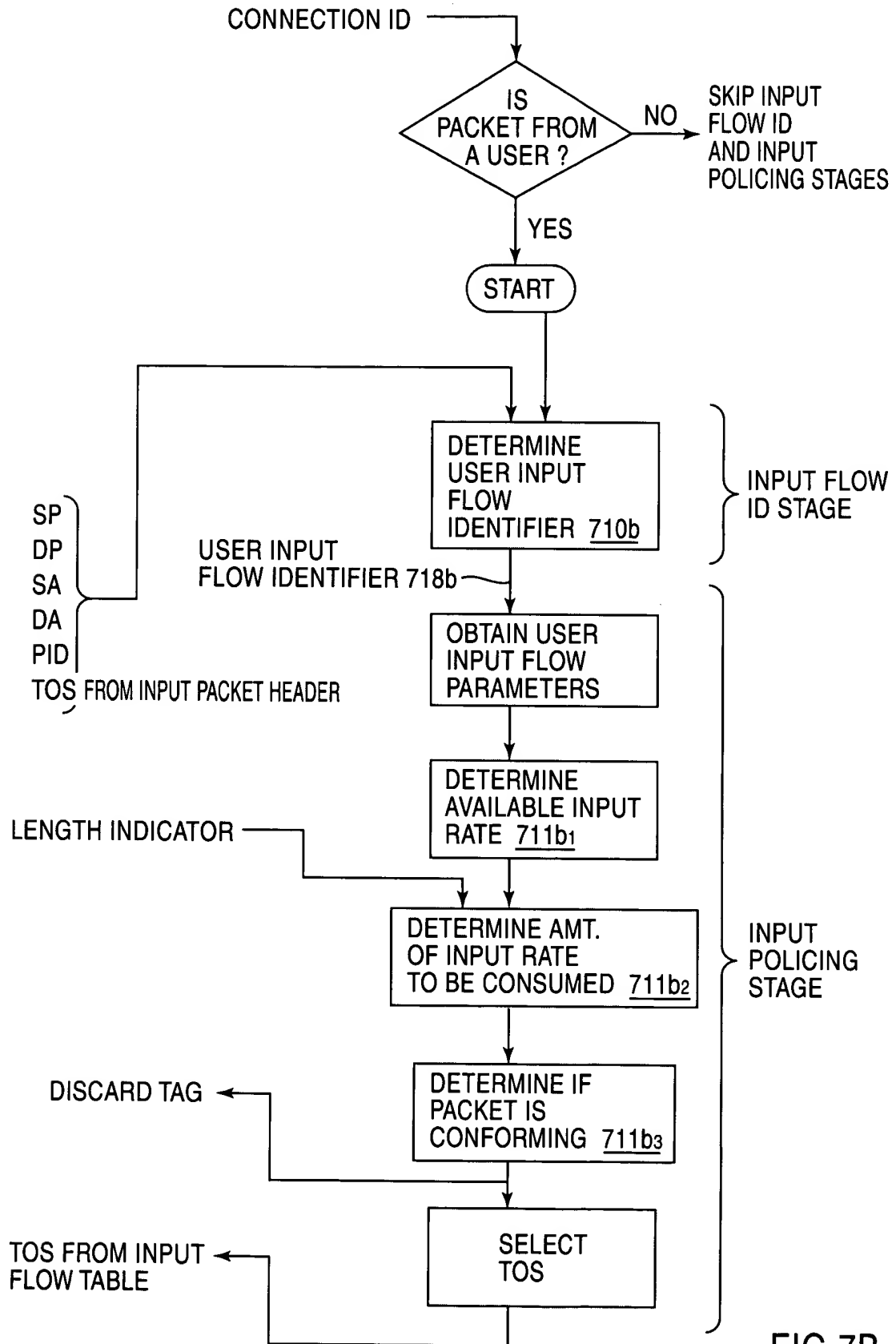


FIG.7B

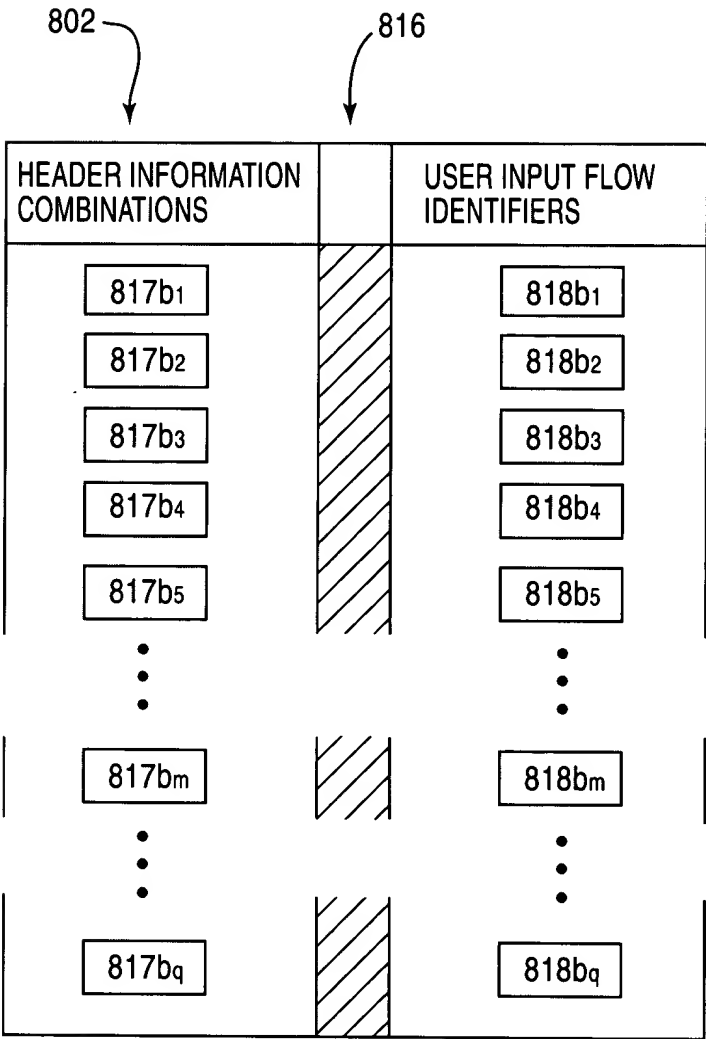
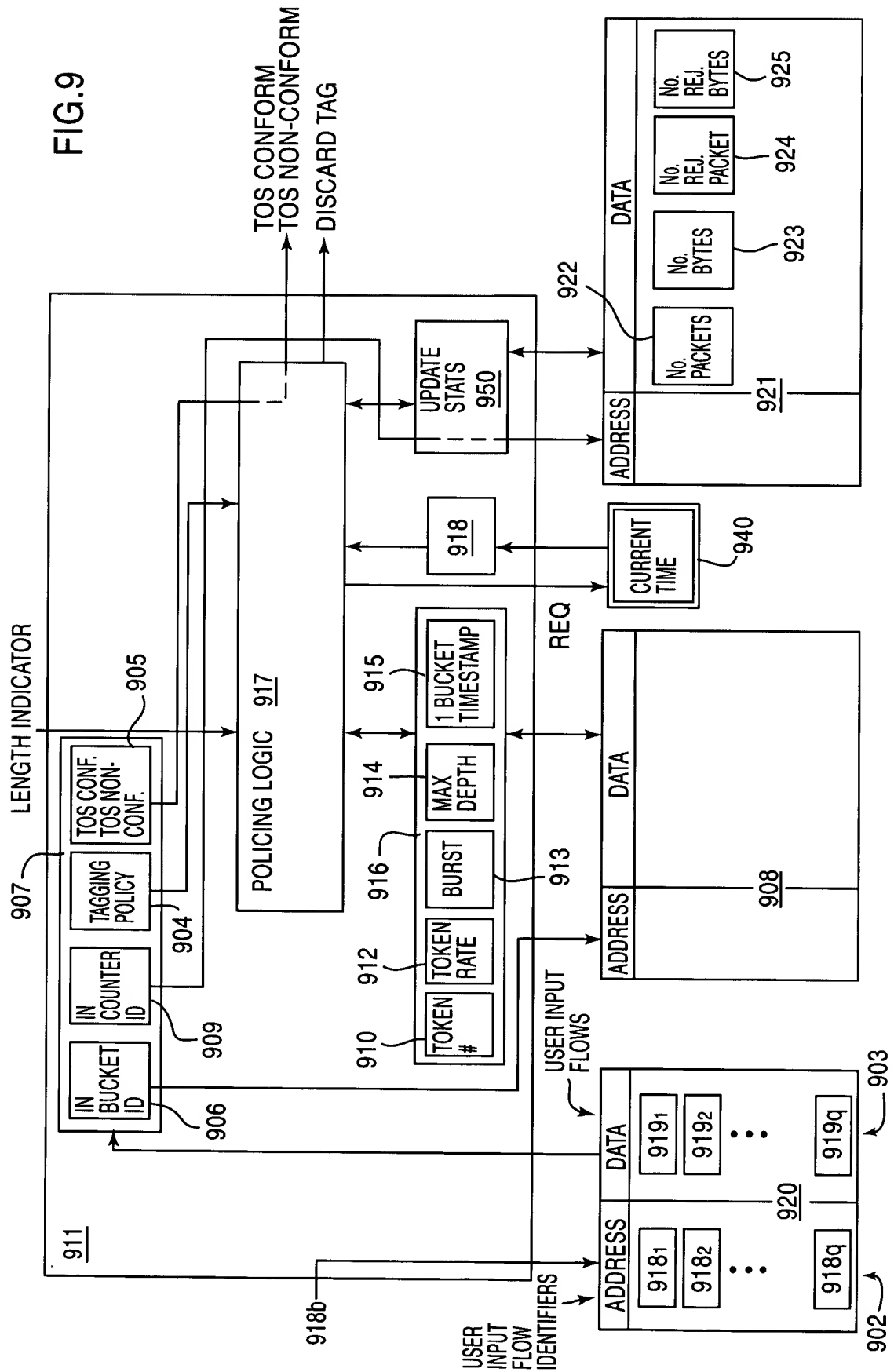


FIG.8



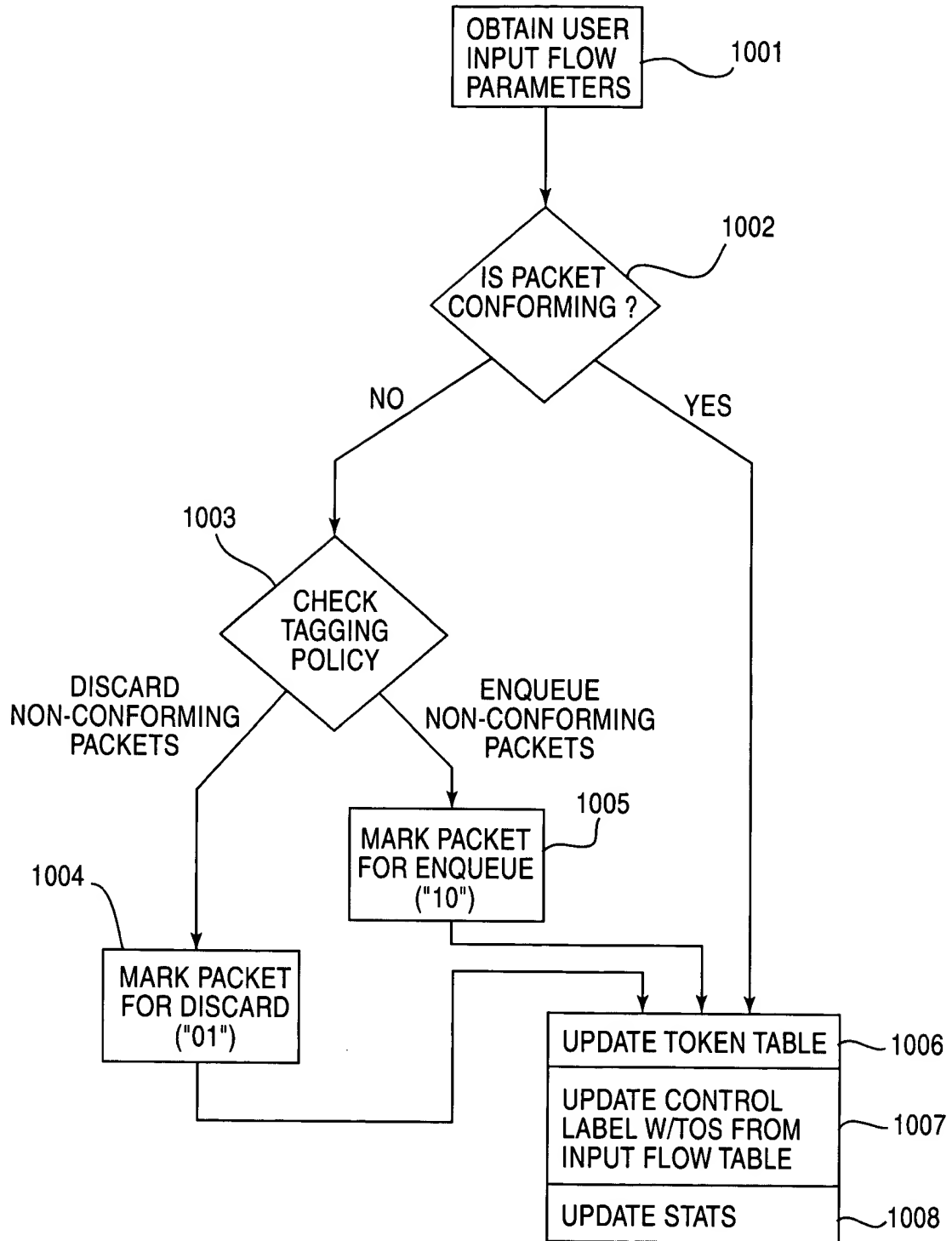
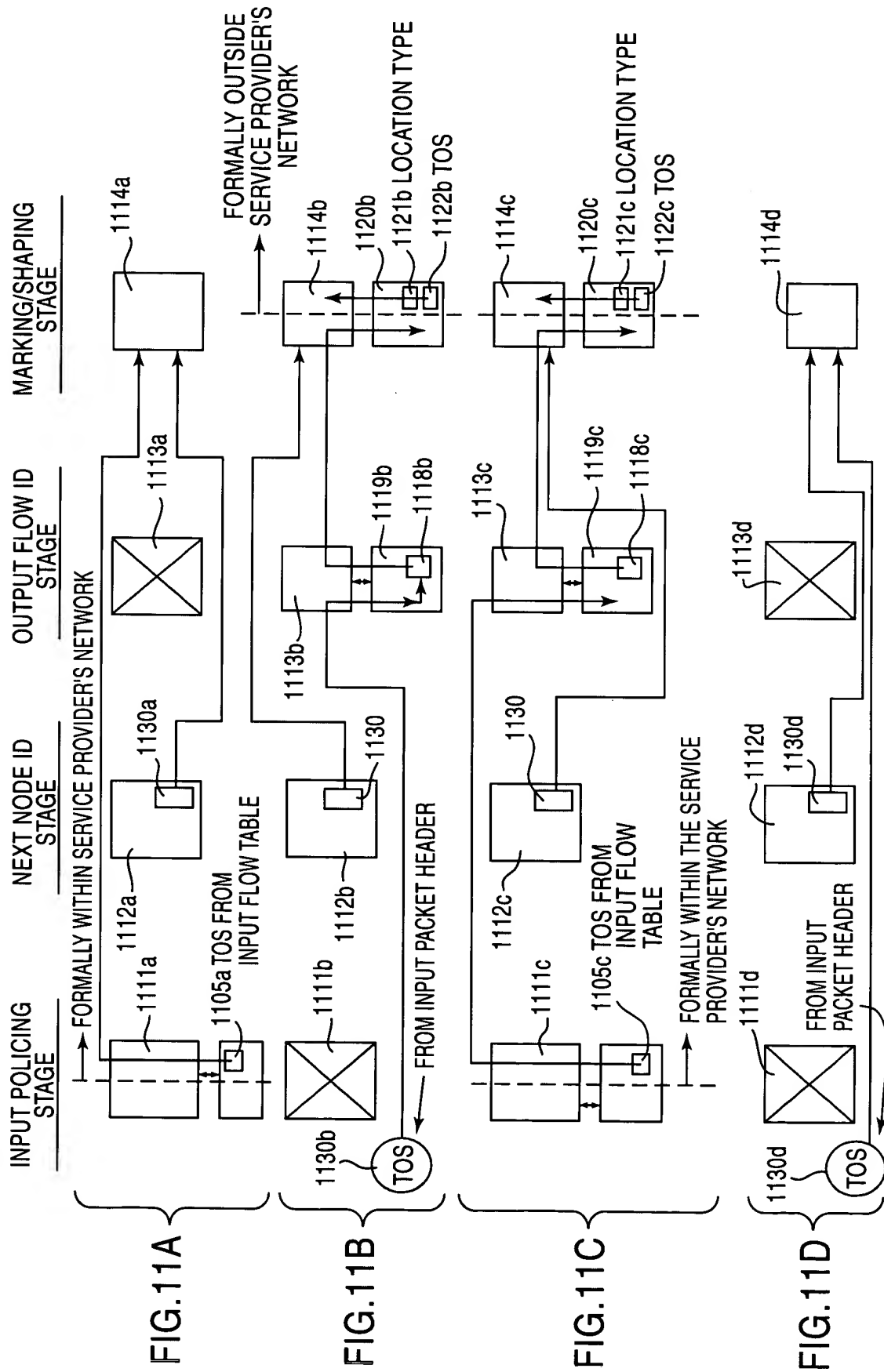


FIG.10



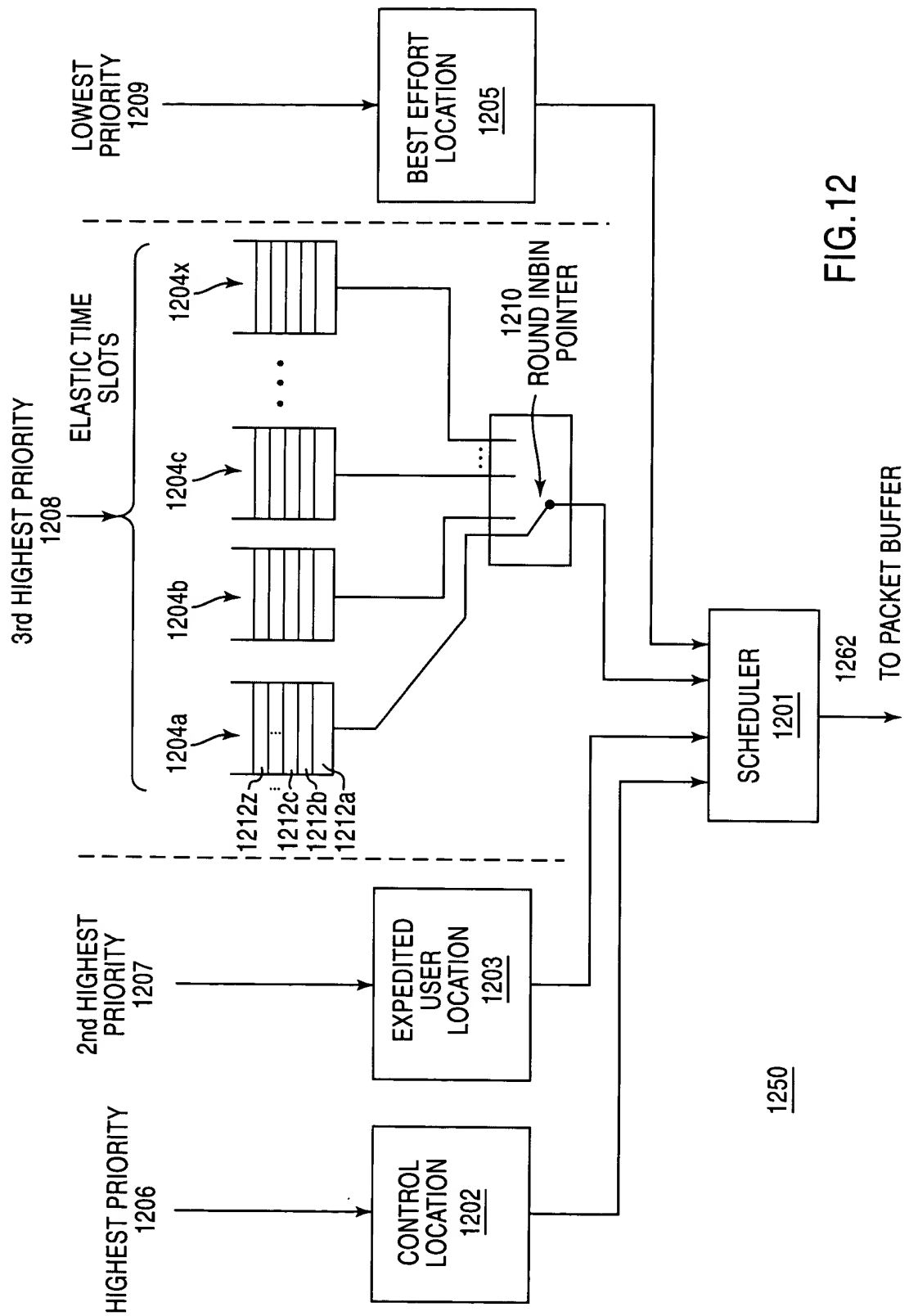


FIG.12

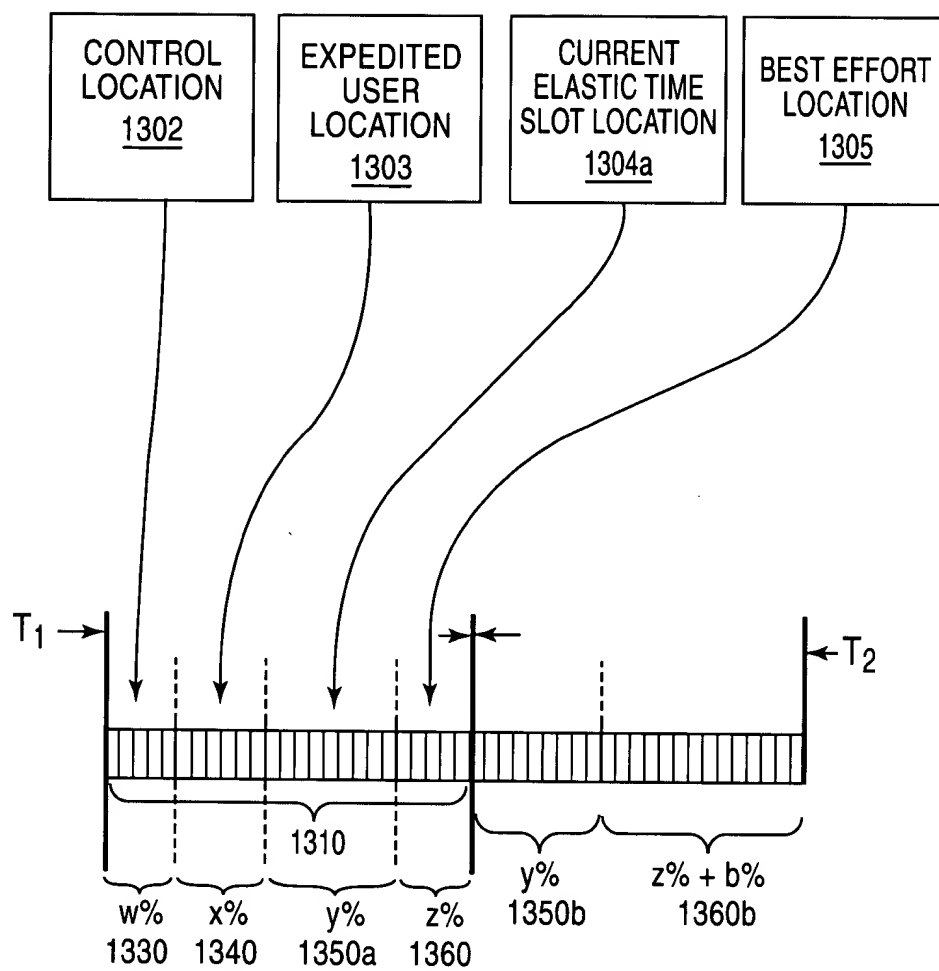


FIG.13

Replacement Sheet

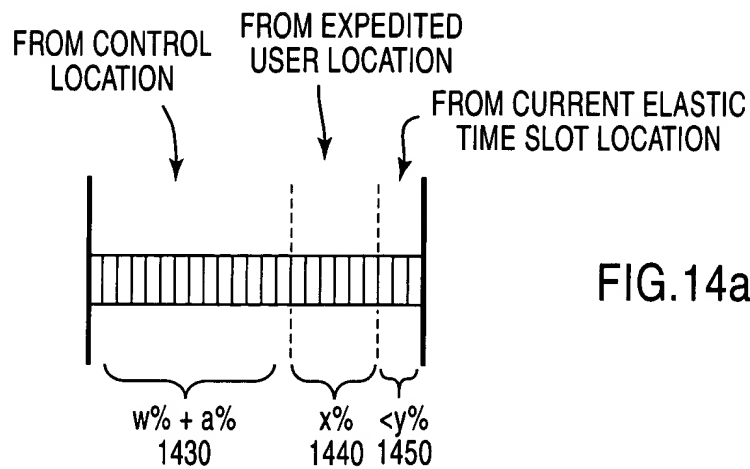


FIG. 14a

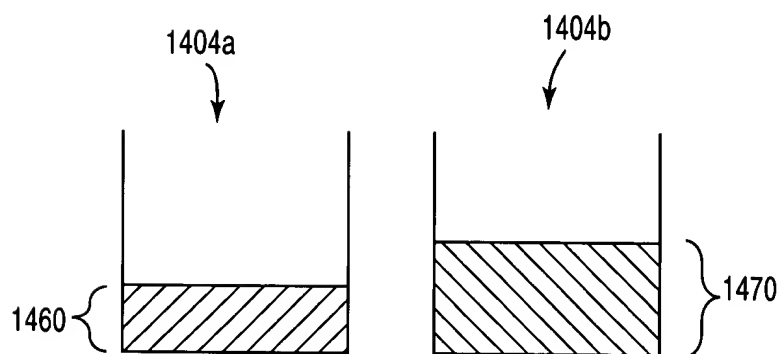


FIG. 14b

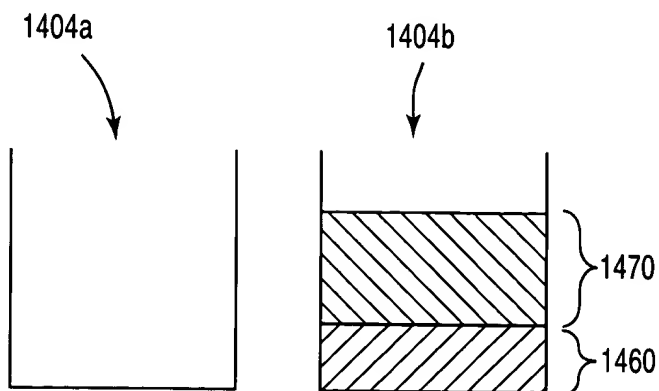


FIG. 14c

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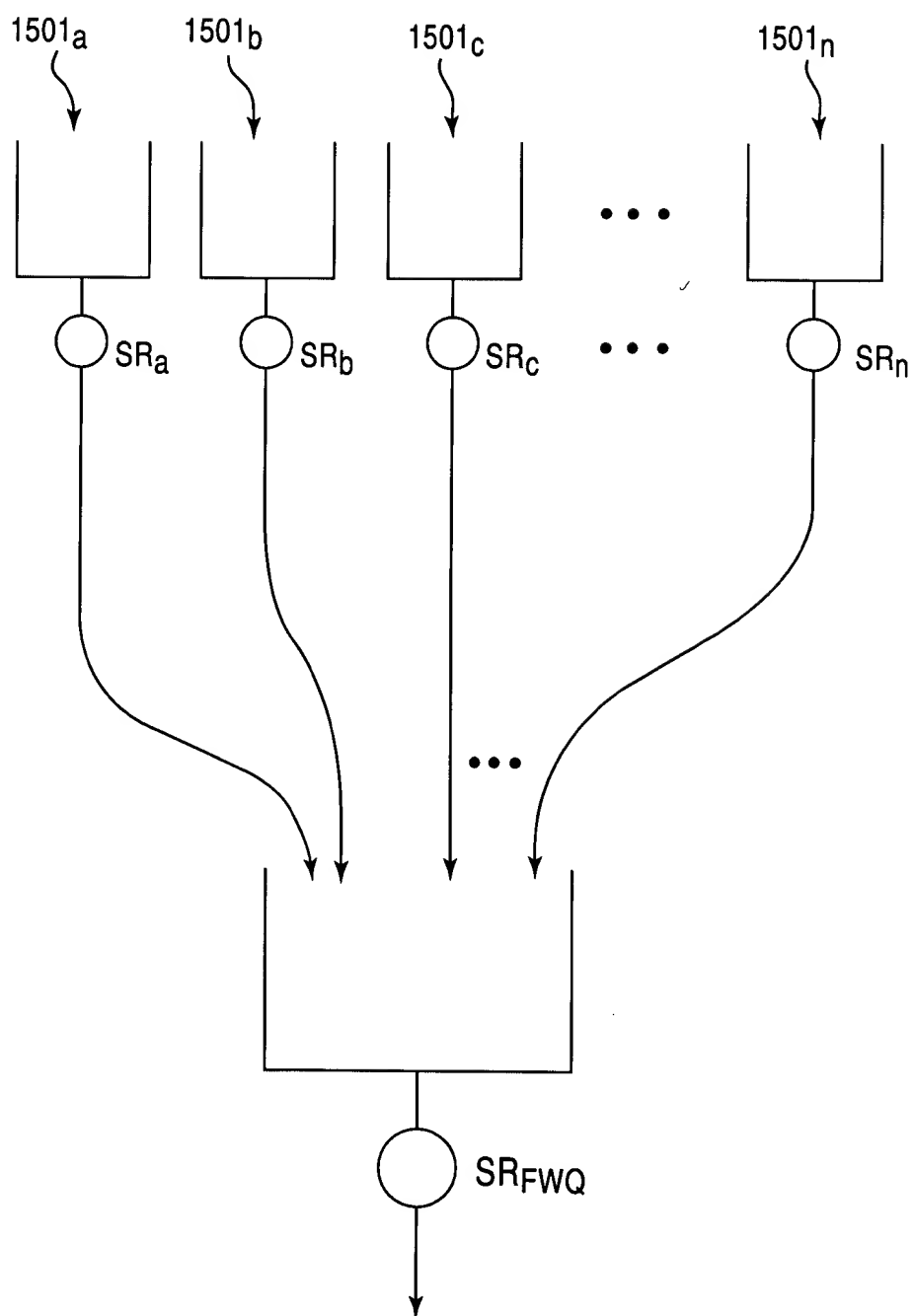


FIG.15

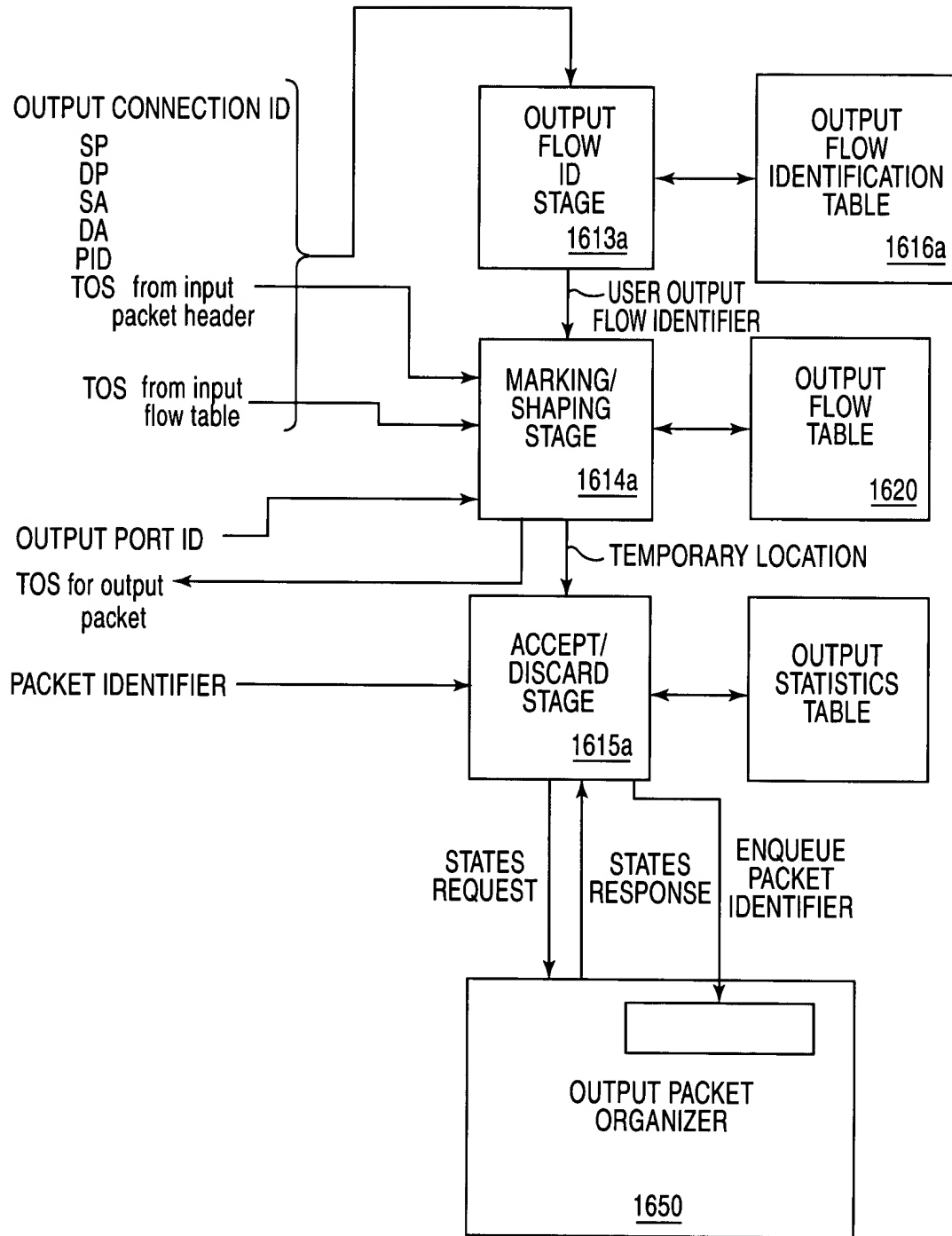
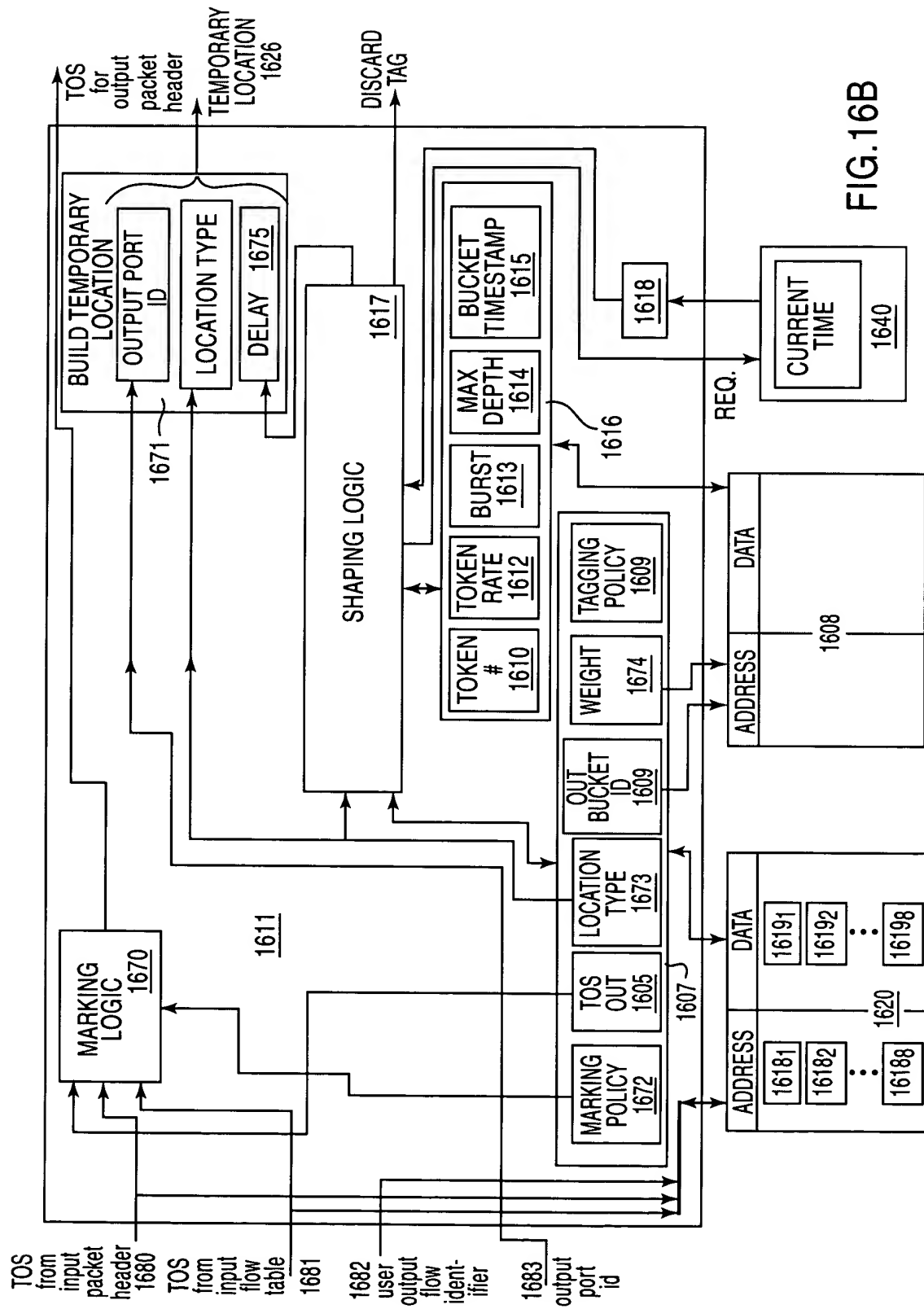


FIG.16a



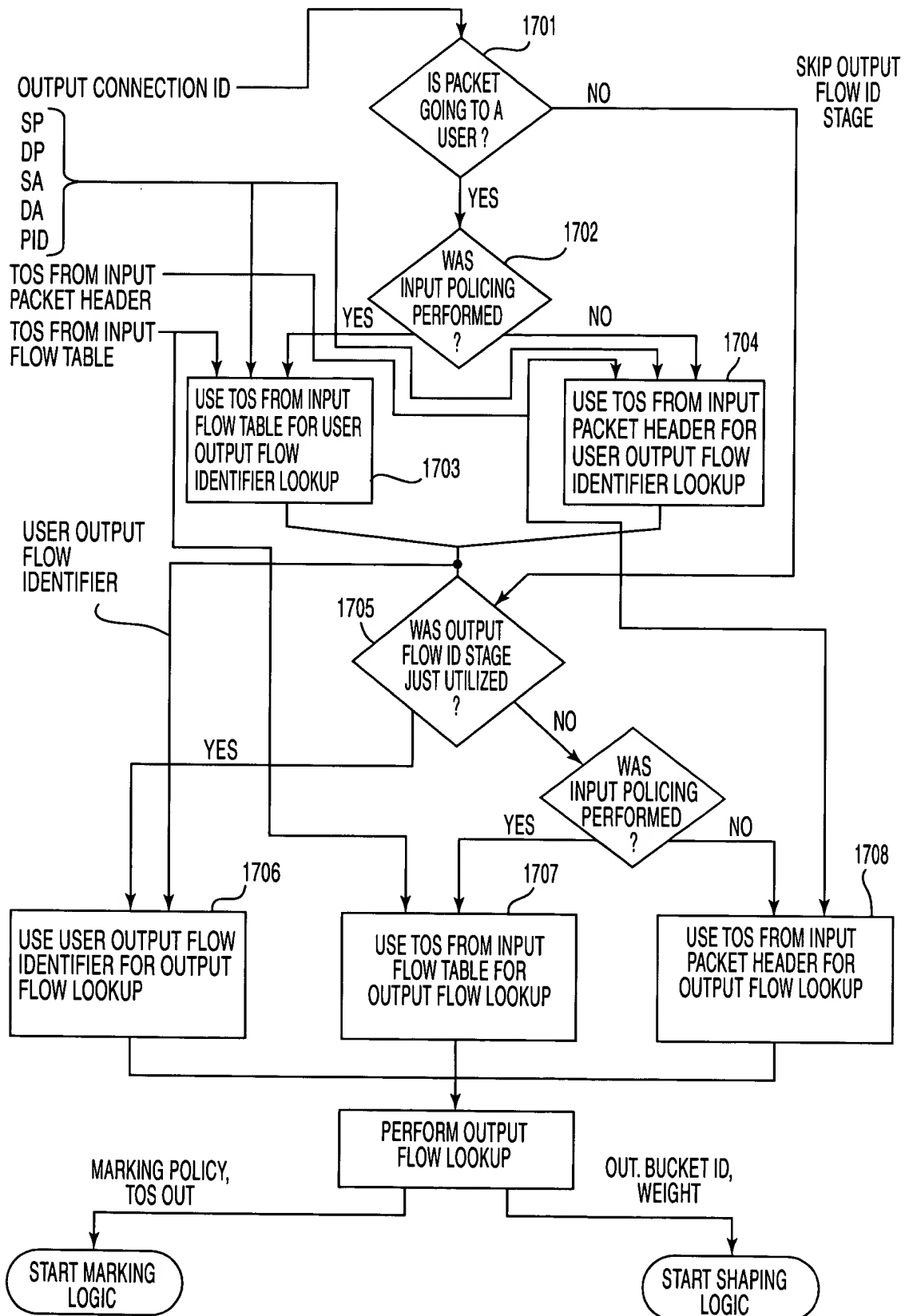


FIG.17a

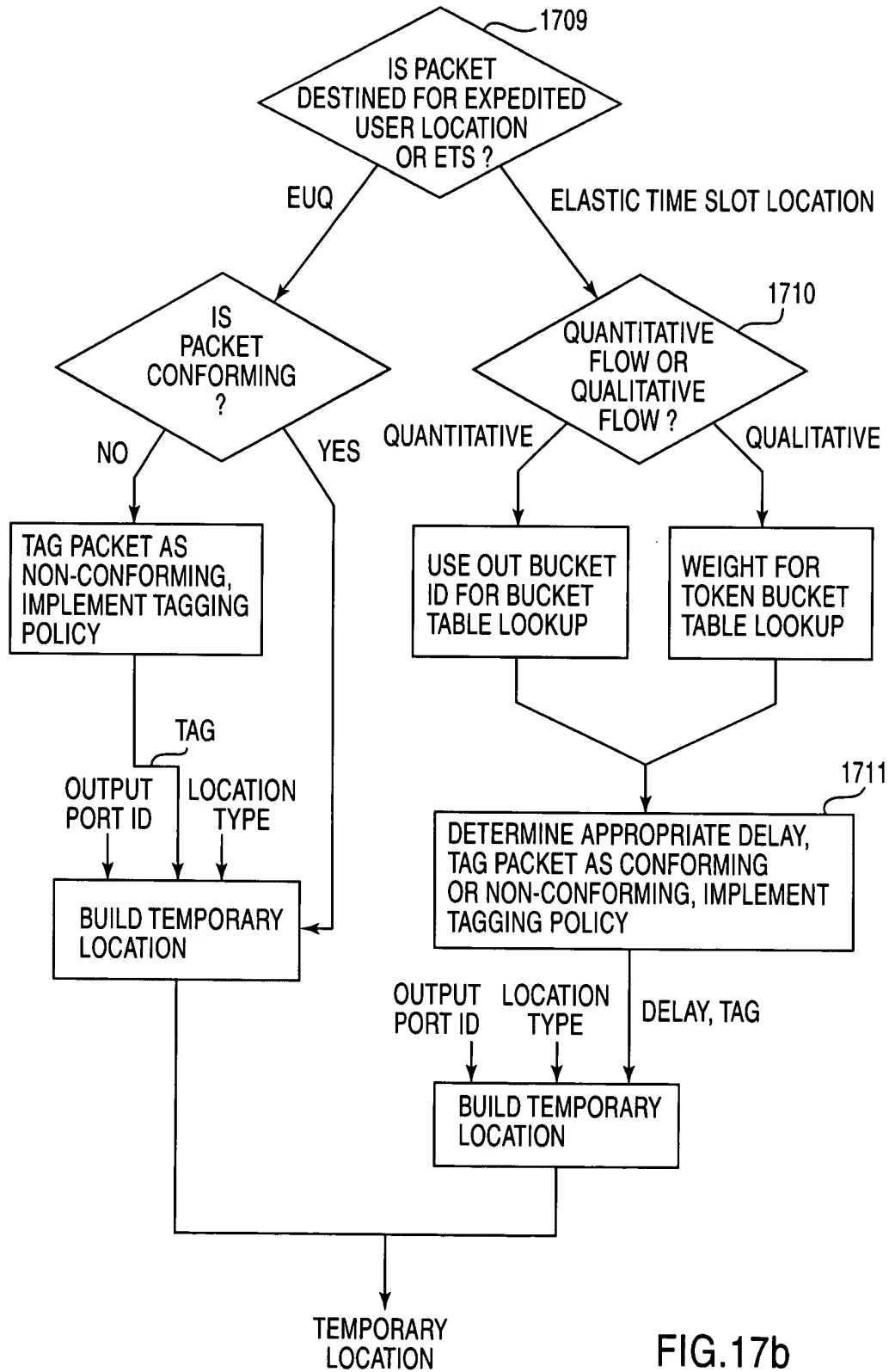


FIG.17b

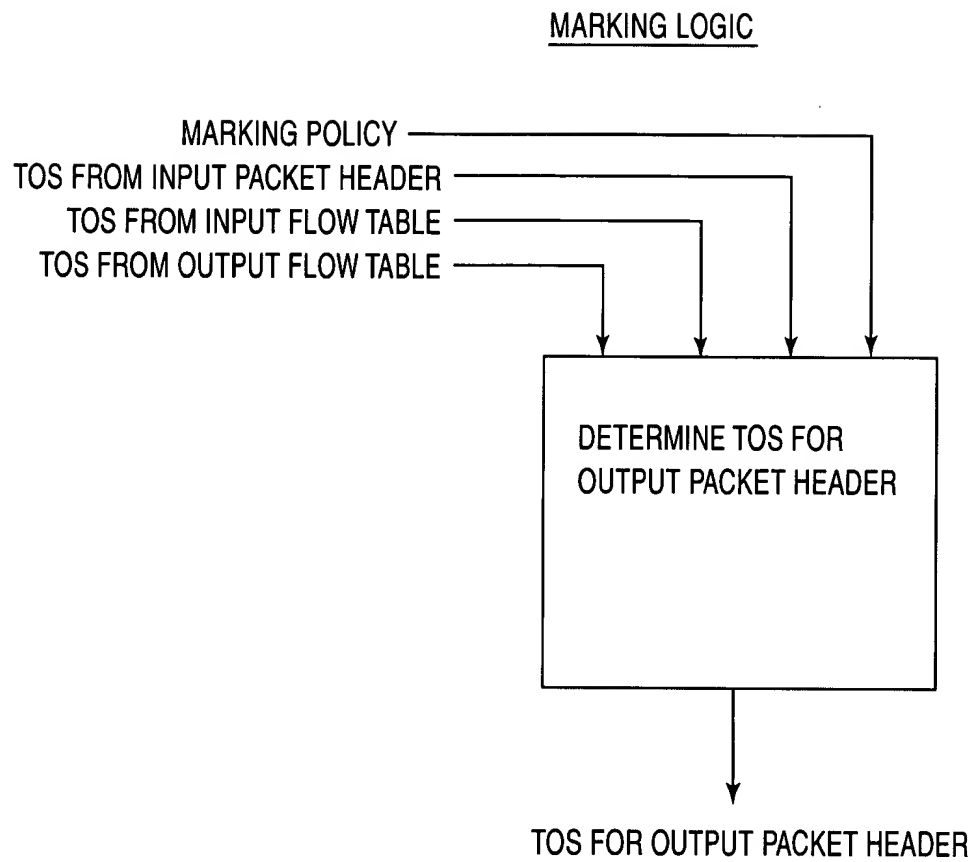


FIG.17c

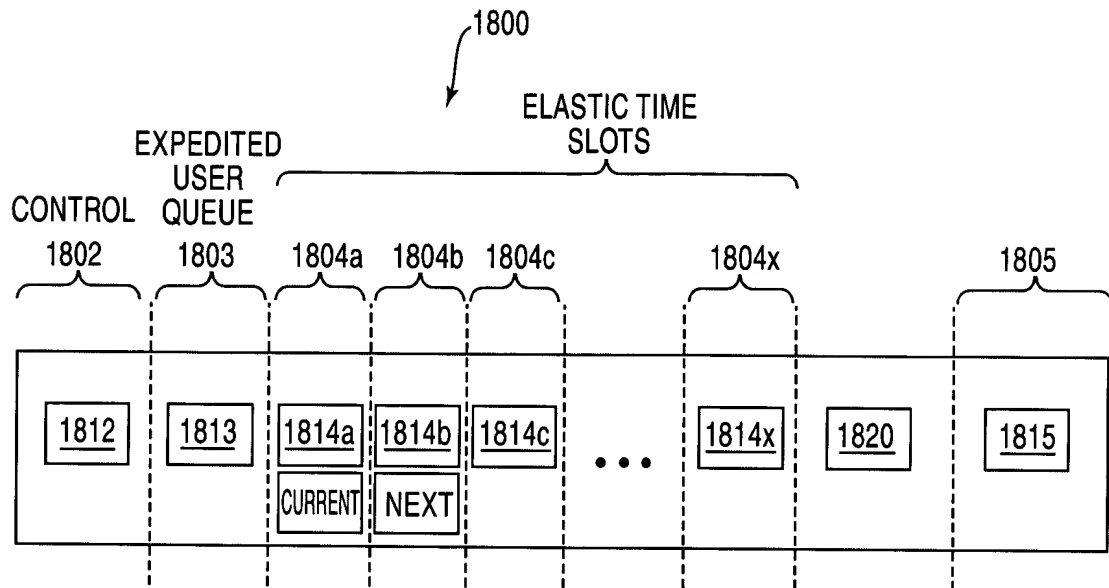


FIG.18